

Art Unit 2189
Serial No.10/633,257

Reply to Office Action of: March 6, 2006
Attorney Docket No.: K35A1307

REMARKS

The Applicant thanks the Examiner for his careful and thoughtful examination of the present application and for the interview granted on May 3, 2006. By way of summary, Claims 1-20 were pending in this application. In this response, the Applicant has canceled Claims 1-20, and prepared new Claims 21-44. Accordingly, Claims 21-44 remain pending for consideration.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

The Office action rejected Claims 1-20 as being indefinite for failing to particularly point out and distinctly claim the subject matter. In particular, the Office action asserted that the claims were unclear because "[h]ow can the invention fetch data stored in the received memory address before a micro-controller request for the data." Although Applicant submits that the claims were correct as previously amended, the new claims have clarified this aspect of the invention, and Claim 21, for example, recites, *inter alia*, that "the micro-controller cache system is responsive to the transmitted address to fetch micro-controller executable data stored at the transmitted address before the micro-controller requests execution of the micro-controller executable data." Accordingly, Applicant respectfully requests withdrawal of the § 112 rejections.

REJECTION OF CLAIMS 1-3, 10-12, 14 AND 17 UNDER 35 U.S.C. § 102(e)

The Office action rejected Claims 1-3, 10-12, 14 and 17 under § 102 as being anticipated by U.S. patent no. 7,000,077, issued to Grimsrud *et al.* (Grimsrud). Applicant has canceled these claims, but respectfully submits that Grimsrud did not anticipate the canceled claims, which were not canceled for reasons related to patentability. Moreover, Applicant submits that Grimsrud fails to identically teach every element of the newly submitted claims 21-44. See M.P.E.P. § 2131 (stating that in order to anticipate a claim, a prior art reference must identically teach every element of the claim).

For example, new Claim 21 recites: a micro-controller cache system responsive to a transmitted address to fetch micro-controller executable data stored at the

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transmitted address before a micro-controller requests execution of the micro-controller executable data. Grimsrud neither teaches nor discloses this limitation.

Instead, Grimsrud teaches a storage system that uses prefetching algorithms to prefetch data from a disk so that the prefetched data can be more efficiently returned to the host. Col. 4, ll. 41-67. The Examiner called out micro-controller 40, in Figure 3, as corresponding to the micro-controller claimed in cancelled Claim 1. Yet, the micro-controller 40 does not request execution of the data returned using the disclosed prefetching algorithms. Instead, this prefetched data is simply forwarded to the host. Thus, Grimsrud does not disclose that the micro-controller cache system fetches micro-controller executable data before the micro-controller requests execution of the micro-controller executable data.

Claim 21 further recites: a cache demand circuit for receiving an address in the remote memory from a micro-controller and transmitting the address to the micro-controller cache system before the micro-controller requests execution of the micro-controller executable data stored at the transmitted address. Grimsrud neither teaches nor discloses this limitation.

The Examiner cited the prefetch algorithms 112 of Grimsrud as corresponding to the cache demand circuit of cancelled Claim 1. Yet, in Grimsrud, a host driver "tells the storage system which demand blocks to read, and gives the storage system the address of the driver's buffer memory. The storage system decides which blocks to prefetch and return with the demand blocks, according to the prefetch algorithms." Col. 6, ll. 20-25 (emphasis added). Thus, the prefetch algorithms 112 taught by Grimsrud use the well-known caching methodology of receiving an address from a micro-controller, and then using that address to prefetch information at one or more prefetch addresses derived from the received address, as discussed in the background of Applicant's specification (p. 1, ll. 22-24). Grimsrud does not teach or suggest a cache demand circuit for receiving an address from a micro-controller and transmitting the address to the micro-controller cache system before the micro-controller requests execution of the micro-controller executable data stored at the transmitted address.

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For at least these reasons, Claim 21 should not be rejected as anticipated by Grimsrud.

New Claim 34 recites: caching micro-controller executable data stored at an address in the micro-controller cache system before the micro-controller requests execution of the micro-controller executable data. Grimsrud neither teaches nor discloses this limitation.

For reasons similar to those discussed above with respect to Claim 21, Applicant submits that Grimsrud neither teaches nor discloses a micro-controller requesting execution of micro-controller executable data.

New Claim 34 further recites: receiving at a cache demand circuit an address in a remote memory from a micro-controller, transmitting the address from the cache demand circuit to the micro-controller cache system, and caching the micro-controller executable data stored at the address before the micro-controller requests execution of the micro-controller executable data.

For reasons similar to those discussed above with respect to Claim 21, Applicant submits that Grimsrud neither teaches nor discloses these steps.

For at least these reasons, Claim 34 should not be rejected as anticipated by Grimsrud.

Claims 22-33, which depend from Claim 21, and Claims 35-44, which depend from Claim 34, are believed to be patentable for at least the same reasons articulated above, and because of the additional features recited therein.

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REJECTION OF CLAIMS 4-9, 13, 15-16 AND 18-20 UNDER 35 U.S.C. § 103(a)

The Office action rejected Claims 4, 8, 13, 15 and 16 under 35 U.S.C. § 103 as being unpatentable over Grimsrud in view of U.S. patent no. 6,789,132, issued to Hoskins (Hoskins). The Office action also rejected Claims 5-7, 9 and 18-20 under 35 U.S.C. § 103 as being unpatentable over Grimsrud, Hoskins, and further in view of U.S. patent no. 6,516,389, issued to Uchihori (Uchihori).

REFERENCES FAIL TO TEACH ALL OF THE CLAIMED ELEMENTS

Applicant has canceled these claims, but respectfully submits that Grimsrud, in view of Hoskins and Uchihori did not render the canceled claims obvious. Moreover, Applicant submits that Grimsrud, alone or in combination with Hoskins and/or Uchihori, fails to teach or suggest all of the elements of the newly presented Claims 21-44. See M.P.E.P. § 2143 (stating that in order to establish a *prima facie* case of obviousness for a claim, the prior art references must teach or suggest all the claim limitations).

The limitations discussed above with reference to Claims 21 and 34 are not taught or suggested by Hoskins or Uchihori. For at least these reasons, Claims 21 and 34 should not be rejected as obvious over Grimsrud, Hoskins and/or Uchihori.

Therefore, Claims 22-33, which depend from Claim 21, and Claims 35-44, which depend from Claim 34, are believed to be patentable for at least the same reasons articulated above, and because of the additional features recited therein.

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CONCLUSION


In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are now in condition for allowance and requests reconsideration of the rejections. If it is believed that a telephone conversation would expedite the prosecution of the present application, or clarify matters with regard to its allowance, the Examiner is invited to contact the undersigned attorney at the number listed below.

The Commissioner is hereby authorized to charge payment of any required fees associated with this Communication or credit any overpayment to Deposit Account No. 23-1209.

Respectfully submitted,

Date: May 26, 2006

By:



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